Job advertisement form

EMPLOYER'S DETAILS

Company/Employer name*:	**Nokia Solutions and Networks Oy, Oulu**
Address*:	**Kaapelitie 4** **90620 Oulu, Finland**
Telephone:	
Website:	https://www.nokia.com/ and https://careers.nokia.com/

Description of the employer*:	Nokia is a global leader in the technologies that connect people and things. With state-of-the-art software, hardware and services for any type of network, Nokia is uniquely positioned to help communication service providers, governments, and large enterprises deliver on the promise of 5G, the Cloud and the Internet of Things. Serving customers in over 100 countries, our research scientists and engineers continue to invent and accelerate new technologies that will increasingly transform the way people and things communicate and connect. Imagine creating technology that has the potential to change the world. With us, you will work with next-generation technology to design products and solutions that will shape the future.

DETAILS AND DESCRIPTION OF THE POSITION

Eures portal ref:	ZmQ0NTU1NjQtZTFmYS00NTU5LWI2NjEtZTBkYjE5MGRkMjFjIDgx
Job title*:	**Implementation Engineer, DFE ASIC** **(in ISCO: 21520 + 21530, 21531)**
Work experience (none – 1 y, 1 – 5 yrs, more than 5 yrs):	**over 5 years**
Number of employees to be recruited*:	**7**
Initial date of employment (date or text)*:	**according to agreement**
Duration of employment (less than 11 days, 11 days – 1 mth, 1 – 3 mths, 3 – 6 mths, 6 – 12 mths, more than 12 mths)*:	**more than 12 months (permanent)**
Working time (full-time/shift work/part-time/night work/weekend work) and number of hours*:	**Full-time**
Salary: (gross or net) (hour/mth/year)	**according to agreement**
Type of employment contract (paid work, commission-based, entrepreneur)*:	**paid work**

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Job description requirements etc*:

About Nokia

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We are looking for SoC Implementation (Synthesis & STA) Engineer to SoC DU organization

Qualifications

We are looking for an engineer interested in SoC Hard Macro & top-level implementation activities. An engineer who is willing to do SoC implementation activities and capable to use the needed tools. A 6+ years of SOC/FPGA implementation experience is expected. In addition, any experience with SoC/FPGA/IP development is considered as an advantage.
You have a hungry mind to learn more and you are excited doing a variety of different kinds of tasks as part of your job. You are always ready to share your knowledge and skills among the people you work with. You are a team worker but also efficient on independent tasks, and your English language skills allow you communicate efficiently in our multicultural environment.

Main Responsibility Area
Basic requirements for implementation specialist are very good understanding and practical experience of synthesis, STA, timing closure and formal verification. The precise job description of the main tasks can be tailored based on your interest and experience.

Job Description:
• Participate in outlining System-on-Chip top-level activities
• Work with various design groups across different disciplines (RTL design, verification, DFT & layout) to meet timing closure, area, power, and performance requirements.
• Perform logic synthesis, logic equivalence checking, static timing analysis, power estimation and hand-off checks using best-in-class methodologies
• Analyze log and report files to ensure the tools are getting the required results.
• Develop the scripts to get the required results within the scheduled milestones
• Advising RTL designers and junior implementation designers related to constraints, timing closure & vendor requirements

Additional Requirements:
• Bachelor's or Master's Degree in Engineering or equivalent
• 6+ years working experience in FPGA/ASIC/SoC development
• Familiar with digital design and UNIX/LINUX environment
• Knowledge of ARM standards, processors and interconnects
• Good understanding of RTL design and RTL requirements for synthesis
• Good experience of scripting languages like TCL, Python, Perl
• Good knowledge of SoC (ASIC/FPGA) implementation tools
• Understanding of Cellular networks and 2G, 3G, LTE and 5G technology
• Fluent spoken and written English

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Beneficial skills:
- Low power understanding
- Experience of DFT, P&R or floorplanning
- Knowhow of packages, thermal, testing, product engineering

additional information	for senior consultants a relocation package is possible
This employment complies with the legislation of FINLAND *	
Contact	**https://careers.nokia.com/**

APPLICATION PROCESS

Deadline for applications*:	**17th September 2021**
Send applications to:	**https://aluperf.referrals.selectminds.com/jobs/implementation-engineer-dfe-asic-61817**